VERAS SYSTEMS F8 KIT
ASSEMBLY INSTRUCTIONS
(similar to Fairchild/Mostek F8 Evaluation Kit)

1) KIT FEATURES:

THE VERAS F8 KIT ASSEMBLED AS INDICATED BY THE ASSEMBLY DRAWING WILL PROVIDE THE FOLLOWING FEATURES:

1024 BYTES OF PROGRAM OR DATA STORAGE AT ADDRESS H'0000' TO H'03FF'

4 I/O PORTS HAVING THE FOLLOWING ADDRESSES:

3850 CPU I/O:	H'00'
	H'01'
3851 PSU I/O:	H'04'
	H'05'

ALL I/O PORTS ARE THE STANDARD CONFIGURATION SUITABLE FOR TTL INTERFACE.

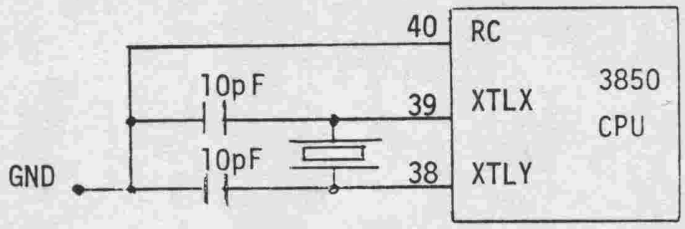
2 LEVELS OF INTERRUPT:

THE FIRST LEVEL IS PROVIDED BY THE 3851 PSU. IT HAS THE HIGHEST PRIORITY BEING THE FIRST IN THE PRIORITY CHAIN. ITS VECTOR ADDRESS IS FIXED AT H'0020' FOR TIMER INTERRUPT AND H'00A0' FOR EXTERNAL INTERRUPT. THE PORT ADDRESS, FOR LOCAL INTERRUPT CONTROL IS H'06'. THE PORT ADDRESS FOR THE TIMER IS H'07'.

The second level is provided by the 3853 MI. It has the lowest priority being last in the priority chain. Its vector address is programmable. The following Port and functions are as follows:

Port Address	Function
H 'OC'	Interrupt vector upper byte
H 'OD'	Interrupt vector lower byte
H 'OE'	Local Interrupt Control
H 'OF'	Timer

- The clock reference frequency circuit shown on the schematic drawing is of the R.C. type. Using the values indicated C = 10 pF and R = 25 KΩ adjustable, a clock frequency in the range of 1.0 to 2 MHZ can be selected. If a more accurate operating frequency is required, an external crystal may be used to select a frequency. Crystal connections are shown below:



An external clock can also be used as reference frequency by connecting clock signal to PIN 38 and GND to PIN 40.

- External Reset: Using a momentary switch connected as indicated, external reset or program restart at zero can be initiated manually.

  In the DEBUG Mode as explained further under FAIR-BUG, the "RESET" function causes an entry in the Debug program instead of a program restart at zero.

- Teletype Interface: A teletype convertor circuit is shown as part of the F8 Kit schematic. This circuit permits to easily interface with a Teletype Mode 33 teleprinter, it provides signals for 4 wire full duplex, 20 MA current loop. The recommended teletype is a Teletype Model 33 ASR with

automatic reader on/off control. See Appendix F for Strapping options and other TTY interfaces. Output data to the TTY is taken from bit Ø of I/O port 4. Input data from the keyboard is input to bit 7 of I/O port 4. A teletype MARK is a logic 1 (A Ø volt level at the I/O port). Baud rate is a function of the software program and can be selected by stapping bit 1 and 2 of I/O port 4 (See Input/ Output section of FAIR-BUG). The connection shown on the Kit schematic diagram (I/O port 4, bit 1 & 2 = open) correspond to a 110 baud rate or 10 CPS.

- Debug Program (FAIR-BUG):

INTRODUCTION

A special Debug ROM 3851A PSU has been developed by Fairchild to provide the F8 Kit user with a convenient and powerful programming debut facility which is used to aid in the development of software on the F8 Kit. This debugging program (FAIR-BUG) provides the user with an interactive system via a teletype terminal. The following capabilities are provided:

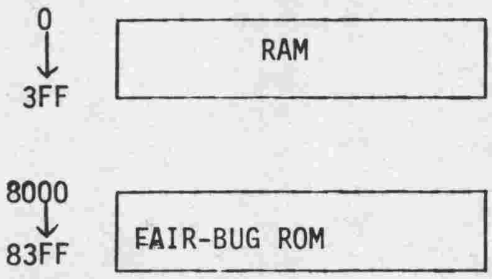
Display or Alter Memory Locations
Display or Alter Scratchpad Registers
Display or Alter Accumulator, ISAR, Status (W Register)
Display or Alter PC0, DC0, DC1
Load Formatted Paper Tape
Punch Formatted Paper Tape
Punch Paper Tape in PROM format
Entry from Keyboard or by Program Instruction
I/O Subroutines available to user

The FAIR-BUG ROM has the memory addresses 8000 - 83FF with the entry point being H'8080'. Input/Output Ports 4 and 5 are also assigned to this ROM. Entry to the debug program is achieved either by depressing the "RESET" switch with the Mode Switch "DEBUG" in the "ON" position or by program instruction PI H'8080'.

FAIR-BUG will save the state of the machine upon entry and will restore it upon return to the users program. Register 8 and PC1 are lost by the syster; however, under program control the user can save and restore these if necessary. The save area utilized by FAIR-BUG is scratchpad registers 3C to 3F and also the last 26 bytes of RAM whose address will either be 3E6 to 3FF or BE6 to BFF. The interrupt is disabled by FAIR-BUG which the user may re-enable if desired.

MEMORY ALLOCATION

The basic F8 Kit system contains 1024 bytes of memory which may be expanded by the user. This memory is organized as shown below:



The FAIR-BUG uses the last 26 bytes of RAM to save the users CPU status. This is address: 3E6 to 3FF

INPUT/OUTPUT

The FAIR-BUG ROM has 2 ports (4 & 5) which are also available to the user when FAIR-BUG is not executing.

Port 4 is used for serial input/output and control functions while Port 5 is used for parallel input data transfer from a high speed paper tape reader. Assignments for Port 4 are:

Bit	Function
7	Serial input
6	Character Ready (Parallel Device)
5	---
4	Device Ready (Parallel Device)
3	Step Reader (Parallel Device)
2 - 1	

bit 2	bit 1	Teletype Baud Rate	Input source during tape load
0	0	110 baud	teletype
0	1	300 baud	teletype
1	0	Baud delay in memory (location 3FF or BFF)	parallel source (port 5)
1	1	Baud delay in memory	teletype

0 = OPEN	Serial Output
1 = GND	

If Port 5 is not utilized by FAIR-BUG, then bits 3, 4, and 6 of Port 4 are also available to the user.

FAIR-BUG parallel read routine examines DEVICE READY and waits for the ready signal, it then looks for Character Ready and delays 100μsec after detecting the ready, then it reads a character before the output of Step Reader. This sequence is repeated for each character. Only the format shown in Appendix B can be read by FAIR-BUG with the Load command. However, the user may use the subroutine PINP to read other formats.

Bits 1-2 are examined when FAIR-BUG is entered to initialize the baud delay counter and also whenever a Load command is given to determine whether the input is bit serial or parallel on Port 5.

FAIR-BUG COMMANDS

When FAIR-BUG is entered a prompt character (?) is sent to the output device. The user then has the option of using any of the debug commands. After each debug execution the user is again prompted with (?). All data and input parameters are in hexidecimal notation. (C/R) following a command indicates a carriage return.

COMMAND TYPE	COMMAND	FUNCTION
Display	A (C/R)	Display the contents of the Accumulator
	DO (C/R)	Display the contents of DCO
	D1 (C/R)	Display the contents of DC1
	I (C/R)	Display the contents of ISAR
	M XXXX (C/R)	Display Memory Location XXXX
	M XXXX-YYYY (C/R)	Display Memory Location XXXX to YYYY
	PO (C/R)	Display the contents of PCO
	P1 (C/R)	Display the contents of PC1
	R XX (C/R)	Display the contents of Register XX
	R XX-YY (C/R)	Display the contents of Registers XX to YY
	S (C/R)	Display the contents of W Register, status
	W (C/R)	Display the contents of W Register, status
Change	C XX (C/R)	Change the previously displayed memory location or register to XX
	C XXXX (C/R)	Change the previously displayed PC or DC to XXXX
Examine	E (C/R)	Display the last addressed register or memory location
Next	N (C/R)	Display the next register or memory location
Load	L (C/R)	Load formatted object paper tape. If (CK) prints then checksum error has occurred on block last read
Punch	B XXXX-YYYY-Z	Binary Punch PROM format XXXX is starting page address and YYYY is ending page address. Z is number of bytes per block 0 = 256, 1 = 512. To punch 0 to BFF then enter B0-C00-0.

COMMAND TYPE	COMMAND	TYPE
	F XXXX-YYYY (C/R)	Formatted punch for future load Manually turn punch to "ON"before issuing the CR .
Go To	G (C/R)	Go to address of PC0
	G AAAA (C/R)	Change PC0 to address AAAA, then go to AAAA to execute next instruction
Delete Command	[	Delete command and start a new command input string

I/O Subroutines on the FAIR=BUG ROM are available to the user. These are listed below and documented in Appendix C.

NAME	ENTRY ADDRESS	FUNCTION
TTYI	83AD	Input 1 byte from TTY type device (11 bits serial/character)
TTYO	83E5	Output 1 byte to TTY type device (11 bits serial/character)
TTCR	83E4	Output CR, LF & Null characters using TTYI subroutine
PINP	8397	Input 1 byte from the parallel IP device (150μsec minimum delay between characters)
FOP1	80EC	Output 1 or 2 hexidecimal digits in ASCII format from register QL
FOP2	80EE	Output 1 or 2 hexidecimal digits in ASCII format from a memory location
BYTE	837B	Input 2 ASCII characters from a parallel or serial IP device; then convert them to one hexidecimal byte

APPENDIX A

FAIR-BUG EXAMPLE 1

```
?M0
 M0000=00
?C 70
?N M0001=91
?C 0B
?N M0002=00
?C 5C
?N  M0003=DD
?C 1F
?N M0004=04
?C 25
?N M0005=10
?C 3F
?N M0006=00
?C 94
?N CF9 M0007=D1
?C F9
?N M0008=00
?C 29
?N M0009=10
?C 80
?N M000A=00
?C 80
?M0-A
 M0000=70 0B 5C 1F 25 3F 94 F9
 M0008=29 80 80 D0 00 10 00 91
?R0-3F
 R0000=A4 FF 09 FF 00 00 FF 00
 R0008=83 0A 00 FF 81 97 03 FF
 R0010=0C 20 13 00 1E 00 BF 00
 R0018=9D 40 7D 01 DD 17 55 00
 R0020=B7 F7 7F A2 FF 0E FF 22
 R0028=FF 76 FF 3C FF CE 5F 20
 R0030=18 04 02 00 D9 04 7F 00
 R0038=75 01 57 4A  F 0A 0A FF
?G0
?M7
 M0007=F9
?C FA
?G0
?R0-3F
 R0000=00 01 02 03 04 05 06 07
 R0008=80 09 0A 0B 0C 0D 0E 0F
 R0010=10 11 12 13 14 15 16 17
 R0018=18 19 1A 1B 1C 1D 1E 1F
 R0020=30 21 22 23 24 25 26 27
 R0028=28 29 2A 2B 2C 2D 2E 2F
 R0030=30 31 32 33 34 35 36 37
 R0038=38 39 3A 3B 3E 09 09 0B
?P0 0000
?P1 EEEE
?M8
 M0008=29
?C28
?G0
?P0 000B
?
```

```
STORE A PROGRAM TO SET
SCRATCHPAD TO 0-3F.

        LIS 0
LOOP    LR  IS,A
        LR  S,A
        INC
        CI  H'3F'
        BNZ LOOP
        JMP H'8080'
```

DISPLAY PROGRAM

DISPLAY SCRATCHPAD
BEFORE EXECUTION

GO TO LOC 0 TO EXECUTE
(PROGRAM LOOP ERR.) MANUAL RESET TO FAIRBUG

CORRECT BNZ INSTRUCTION
GO TO 0

DISPLAY REGISTERS AFTER
EXECUTION.
NOTE: R8, R3C-3F ARE USED
BY FAIRBUG.

PC NOT SAVED BY JMP.

CHANGE JMP TO P1

EXECUTE AGAIN
PC NOW SAVED!

APPENDIX A

FAIR-BUG EXAMPLE 2

```
 R5
 R0005=00
?R1-2
 R0000=A4 FF 09 00 00 00 FF 00
?N R0008=83
?C55
?E R0008=55
?R8
 R0008=55
?P0 83B0
?D0 807B
?D1 0000
?CFFFF
?E FFFF
?D1 FFFF
?I=0F
?S=0A
?W=0A
?M3E0-3FF
 M03E0=04 00 00 10 00 00 00 83
 M03E8=B0 EE EE 80 7B FF FF A4
 M03F0=FF 09 00 00 00 FF 00 55
 M03F8=0A 00 FF 81 97 03 FF 00
?R0-F
 R0000=A4 FF 09 00 00 00 FF 00
 R0008=55 )A 00 FF 81 97 03 FF
?R10-40
 R0010=00 20 13 00 1E 00 BF 00
 R0018=9D 40 7D 01 DD 17 55 00
 R0020=B7 F7 7F A2 FF 03 FF 22
 R0028=FF 76 FF 3C FF CE 5F 20
 R0030=18 04 02 00 D9 04 7F 00
 R0038=75 01 57 4A 0F 0A 0A FF
 R0040=A4 FF 00 00 44 00 47 EF
?B0-100-00F0B0N0B0N0B0N0F0M0F0N0F000BNN0BMBM@0@0@M@0CM@M@M@0@MA0@MB0@0FM@NN0BL

?F0-FFS0000
X009100DD041000D17
X001000D0001000919
X0010009000100090 4
X000000D1141002D47

X24DA20C1AFFB20FFF
X26C802F3268164FBD
X20D900FF24F900F9C
X26F900FF2ED92EF58
*
?F0-FF
?A=83
?C00
?E R0008=00
?N R0009=0F
?G8080
?PC 00FF
?P0 8080
?G
?
```

R1-2 TYPES R0-R7

NEXT=R8
CHANGE R8 TO 55
EXAMINE R8

DISPLAY DC1, CHANGE, EXAMINE,
THEN DISPLAY AGAIN

ISAR

STATUS

MEMORY DUMP

REGISTER DUMP

REGISTER DUMP

NOTE: R40-R47 IS FAIRBUG USE

PUNCH FORMAT (PROM TAPE)
SEE APPENDIX C FOR FORMAT
PUNCH FORMAT (LOAD TAPE)

SEE APPENDIX B FOR FORMAT

* (END OF TAPE)

DISPLAY, CHANGE, EXAMINE ACCUMULATOR

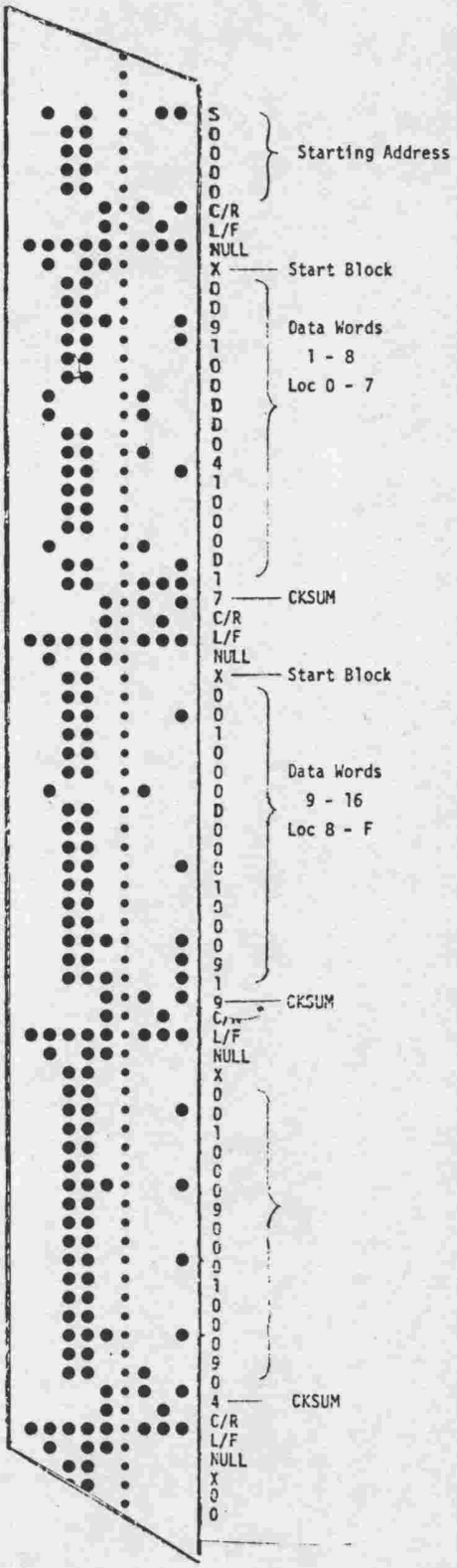
NOTE: ACCUMULATOR IS IN R8 THEREFORE NEXT IS R9
GO TO 8080

PC0 CHANGED TO 8080
GO TO PC0 (8080)

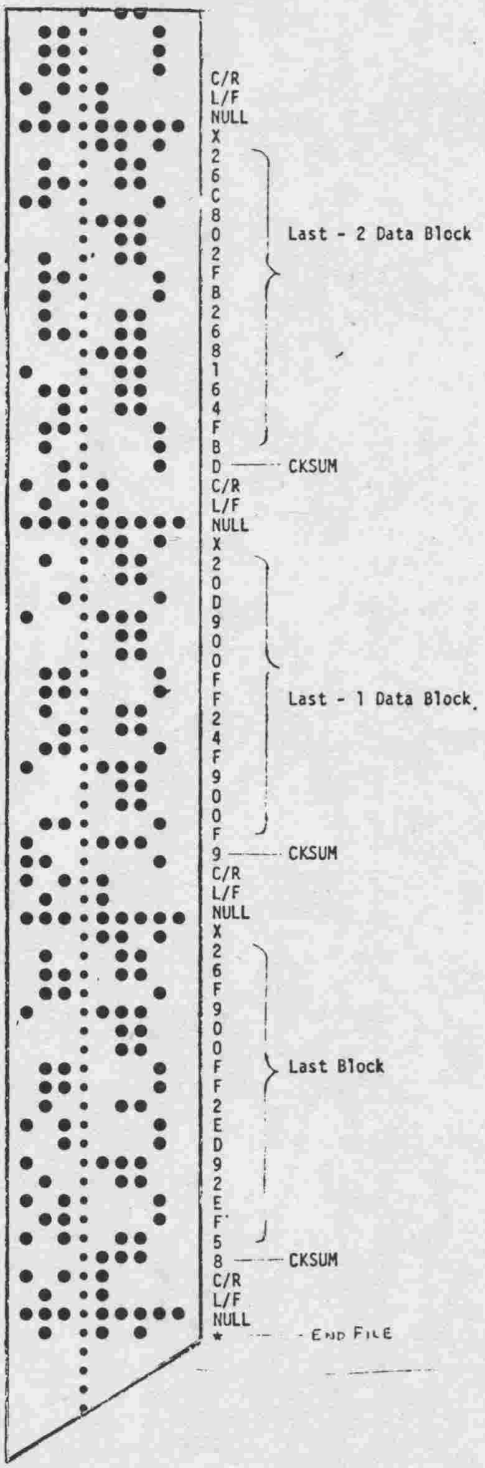
APPENDIX B

FORMATTED TAPE

(LOADER FORMAT)



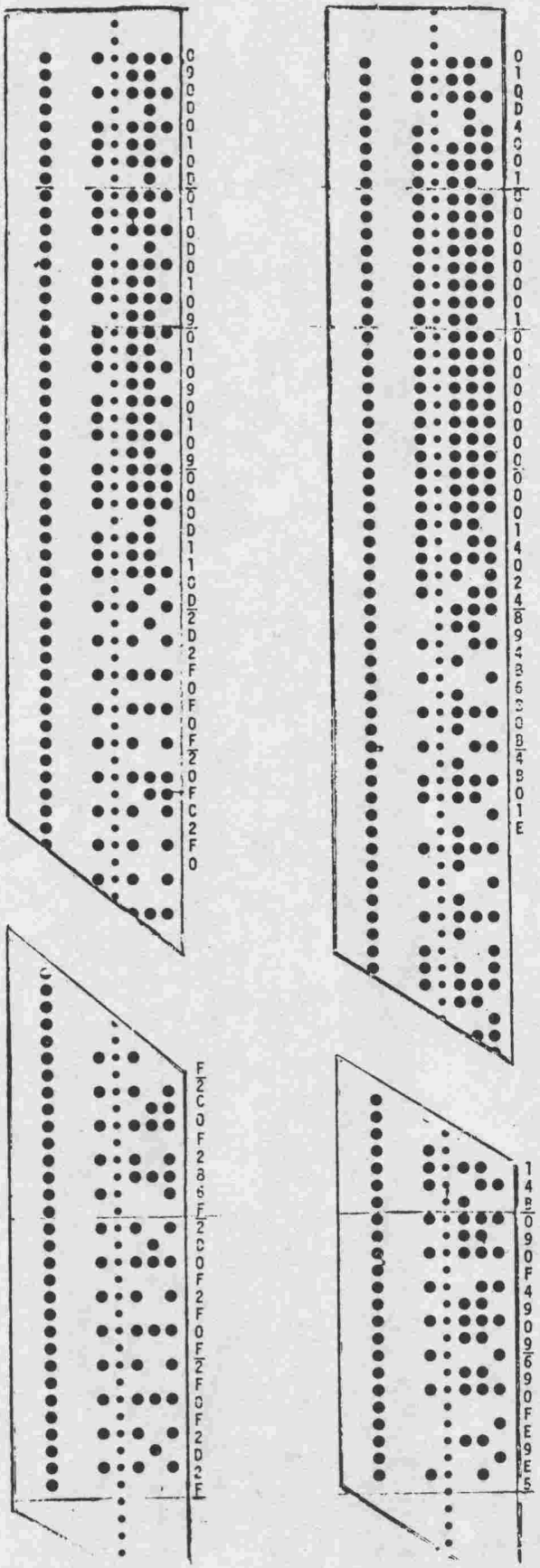
Note: This example was punched by the instruction shown in Appendix B (F0-FF). This is ASCII 7 bit format.



APPENDIX C

BINARY FORMAT

(PROM GENERATION FORMAT)



Note: This example was punched by the instruction shown in Appendix B (B-100-0).

Only the low order 4 bits are significant and are punched in compliment form.

The first block is punched with 256 memory locations hi order bits. The next block has 256 memory locations low order bits.

Subsequent blocks then alternate hi, low, hi, low, etc. with a blank gap between.

The table below shows examples of commands and the results produced.

Input Command B-XX00-YY00-L		Decimal Memory Addresses Punched	# Blocks	Block Length
B	0-100-0	0-255	2	256
B	0-400-0	0-1023	8	256
B	100-200-0	256-511	2	256
B	0-400-1	0-1023	4	512
B	0-1000-1	0-4095	16	512
B	200-400-1	512-1023	2	512

APPENDIX D
FAIR-BUG SUBROUTINES

The following INPUT and OUTPUT subroutines exist in FAIR-BUG and may be called by the users program. All subroutines may be entered by: (PI Address).

TTYI - Input 1 Byte from TTY type device, without echo. Data is 11 bits/character being received on Port 4 Pin 7.

```
Address:  H'83AD'
Enter:    R0 - Delay Counter
Exit:     W Reg - Destroyed
          PC1 - User return address
          Accum - Input byte
          R0 - Unchanged
          R1 - Input byte
          R2 - -1
```

TTY0 - Output 1 byte to TTY type device. Data transmitted is 11 bits/character being output on Port 4 Pin 0.

```
Address:  H'83E5'
Enter:    R0 - Delay Counter
          R1 - Byte to output
Exit:     W Reg - Destroyed
          PC1 - User return address
          Accum - 0
          R0 - Unchanged
          R1 - -1
          R2 - 0
```

TTCR - Output CR/LF/NULL to TTY type device; subroutine TTY0 is called.

```
Address:  H'83D6'
Enter:    R0 - Delay Counter
Exit:     W Reg - Destroyed
          PC1 - H'83E4'
          Accum - 0
          K Reg - User return address
          R0 - Unchanged
          R1 - -1
          R2 - 0
```

PINP - Input 1 byte from parallel input device; minimum delay between characters is 150μsec. Byte is received on Port 5 with control bits on Port 4, pins 3, 4, and 6.

```
Address:  H'8397'
Enter:    No setup
Exit:     W Reg - Destroyed
          PC1 - User return address
          Accum - Input byte
          R1 - Input byte
```

BYTE - Input 2 ASCII hexidecimal characters and convert to 1 byte; also accumulate the checksum. If input is not ASCII characters 0-9 or A-F meaningless results will be returned. Either TTYI or PINP is called as input routine.

Address: H'837B'
Enter: Q - H'8397' (for parallel input)
Q - H'83AD' (serial input) R0 = Delay Counter
R7 - Previously accumulated checksum
Exit: W Reg - Destroyed
PC1 - Destroyed
Accum - Input byte
K - User return address
Q - Unchanged
R0 - Unchanged
R1 - Destroyed
R2 - -1 (if serial IP), unchanged for parallel IP
R7 - Checksum
R8 - 0
R11 - Input byte

FOP1 - Output byte of data from memory to TTY type device using TTYO subroutine. Byte is converted to 1 or 2 ASCII hexidecimal characters.

Address: H'80EC'
Enter: R0 - Delay Counter
R8 - Flag Pos# = OP Hi 4 bits, then Lo 4 as ASCII
Neg# = OP Lo 4 bits as ASCII
DC0 - Memory address of data
Exit: W Reg - Destroyed
PC1 - Destroyed
Accum - Destroyed
DC0 - DC0 + 1
K Reg - User return address
QL - Data byte
R0 - Unchanged
R1 - -1
R2 - 0
R7 - Checksum (low 4 bits significant)

FOP2 - Output byte of data from QL. Same routine as FOP1 except DC0 is not used.

Address: H'80EE'
Enter: R0 - Delay Counter
R8 - Same as FOP1
QL - Data byte to output
Exit: Same as FOP1

APPENDIX E
ASCII CHARACTER CODES

Character	7 Bit Hex Code	Character	7 Bit Hex Code	Character	7 Bit Hex Code
(Space)	20	0	30	H	48
!	21	1	31	I	49
"	22	2	32	J	4A
#	23	3	33	K	4B
$	24	4	34	L	4C
%	25	5	35	M	4D
&	26	6	36	N	4E
' (Quote)	27	7	37	O	4F
(	28	8	38	P	50
)	29	9	39	Q	51
*	2A	:	3A	R	52
+	2B	;	3B	S	53
, (Comma)	2C	>	3C	T	54
-	2D	=	3D	U	55
.	2E	<	3E	V	56
/	2F	?	3F	W	57
		@	40	X	58
Line Feed	0A	A	41	Y	59
Carriage RTN	0D	B	42	Z	5A
Bell	87	C	43	[	5B
Punch ON	92	D	44	\	5C
Punch OFF	94	E	45	]	5D
Reader ON	91	F	46	↑	5E
Reader OFF	93	G	47	←	5F
Null	7F				
Null	FF				

APPENDIX F: Connecting a Teletype Model 33

The F8 Kit system can easily interface with a Teletype Model 33 teleprinter. The teletype convertor of the micromodule provides signals for a 20 mA full duplex loop.

The recommended teletype is a Teletype Model 33 ASR with automatic reader on/off control. Other Model 33 Teleprinters can also be used.

Teletype Strapping Options

No modifications of the teletype are necessary. Strapping options should be selected to provide 20 mA loop currents in place of 60 mA loops, and to provide full duplex operation in place of half duplex operation. The options are described in the following paragraphs:

1. Parts location: All option points are on the teletype power supply assembly. The power supply assembly is rightmost in the teletype; prominent are the LINE/OFF/LOCAL switch in the front of it, and a row of three fuse holders in the rear. Changes are made on a ten terminal strip (part #151411) that is at the lower rear of the power supply assembly. The other change is made on a large flat multi-tap power resistor (part #181816) that is about three inches behind the LINE/OFF/LOCAL switch.

2. Select 20 mA loop currents by performing Note 2 of the TTY Drawing Number 6353WD which states: "For the .020 amp neutral signal line move the purple wire from Terminal 8 to Terminal 9 of the 151411 terminal strip. Also move the blue wire from Terminal 3 of the power resistor 181816 to Terminal 4."

3. Select full duplex operation by performing Note 3 of TTY Drawing Number 6353WD which states: "Move the white-blue wire from Terminal 4 to 5 and the brown-yellow wire from Terminal 3 to 5 on the 151411 terminal strip."

   Caution: The 110V line cord terminates on the terminal strip. Unplug power cord from the AC source before working on the teletype.

Teletype Model 33 machines provide two alternative places for attaching an interface cable. One location is the 10 terminal strip that is at the rear of the power supply assembly (the same place as where the option changes were made). The optional location is at the 15 pin connector #2 which is just above the terminal strip. One mating plug for connector is:

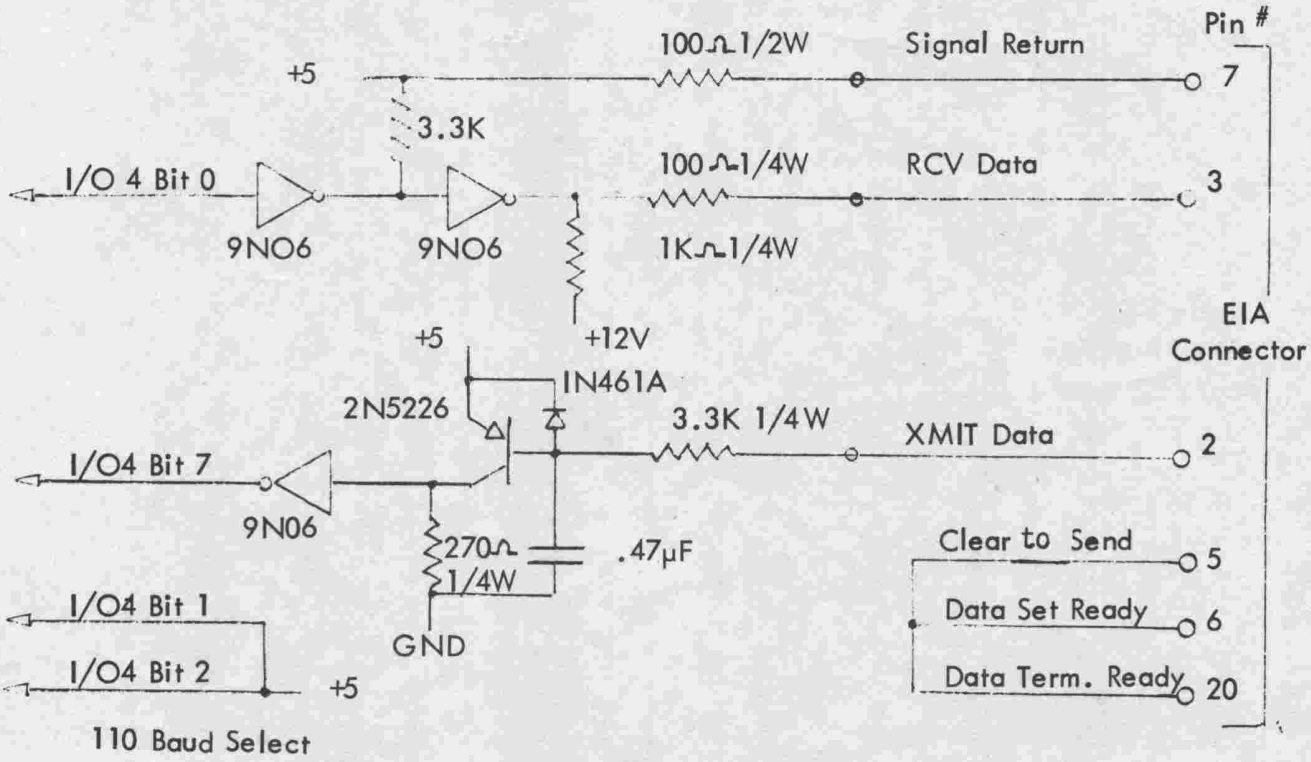
MOLEX part # P(03-09-2151) housing
with MOLEX part # (02-09-2118) terminals

The connections between Teletype and micromodule are:

Teletype	F8 Kit
TS-4 or J2-6	Keyboard
TS-3 or J2-5	Keyboard Return
TS-7 or J2-8	Printer
TS-6 or J2-7	Printer Return

EIA INTERFACE

The following schematic shows alternate TTY convertor circuit for interface with an EIA connector.



1.0 Installation (SEE CPU BOARD ASSY DRAWING)

The Veras F8 kit has 4 sets of 8 bit I/O ports. These 32 pins plus two interrupt inputs are brought out to a standard double sided 22 pin PC edge connector (44 connections total). Also on the connector are the power supply voltages & the teletype adaptor connections. Table 1 gives the pin assignments for the connector. The connector is: Amphenol 225-2221-401 or equivalent.

1.1 Power Requirements: +12V + 5% @ 50mA max- pin-N

+5V + 5% @ 1/2 AMP max- pin A

Gnd ----- - pin Z

1.2 Teletype Connections: The ttl level signals must be tied to I/O port 4 of the 3851A PSU the 44 pin connector:

connector pin 10 to pin 14
pin 12 to pin 15

	110 Baud	300 Baud	Select Baud
Pin 16	open	GND	GND
Pin 17	Open	open	GND

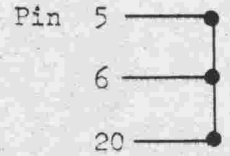
Connections to the teletype are:

Teletype	Name	Kit Connection
TS-4 or J2-6	Keyboard	pin 13
TS-3 or J2-5	Keyboard Return	pin 1
TS-7 or J-28	Printer	pin M
TS-6 or J2-7	Printer Return	pin 2

Teletype should be strapped for 20 ma full duplex operation-- this is the strapping most commonly encountered.

1.3 RS-232 CONNECTIONS

RS-232 connection	NAME	KIT Connection
7	Signal Return	M (PNTR)
3	Received data	2 (PNTR RTRN)
2	Xmit data	13 (KYBRD)
Pin 5	Clear to send	_____
6	Data set ready	_____
20	Data terminal ready	_____



1.4 MEMORY EXPANSION CONNECTION

A 44 pin connector is provided on one end of the PC board that give access to signals needed to expand the RAM by adding additional 2102 memory banks. The signals available are;

16 bits of ADDRESS	AD0-AD15
8 bits of WRITE data:	PI-P8
8 bits of READ data:	DB0-DB7
READ/WRITE	P10

2.0 Operation

The operating controls are the RESET switch (SI) and the toggle DEBUG switch (S2).

To enter FAIRBUG operating system, put toggle switch towards the RESET switch then push & release RESET (toggle switch closed).

To start a program from RAM location 0000: put toggle switch away from RESET switch then push & release RESET (toggle switch open).

TABLE 1 (J1)

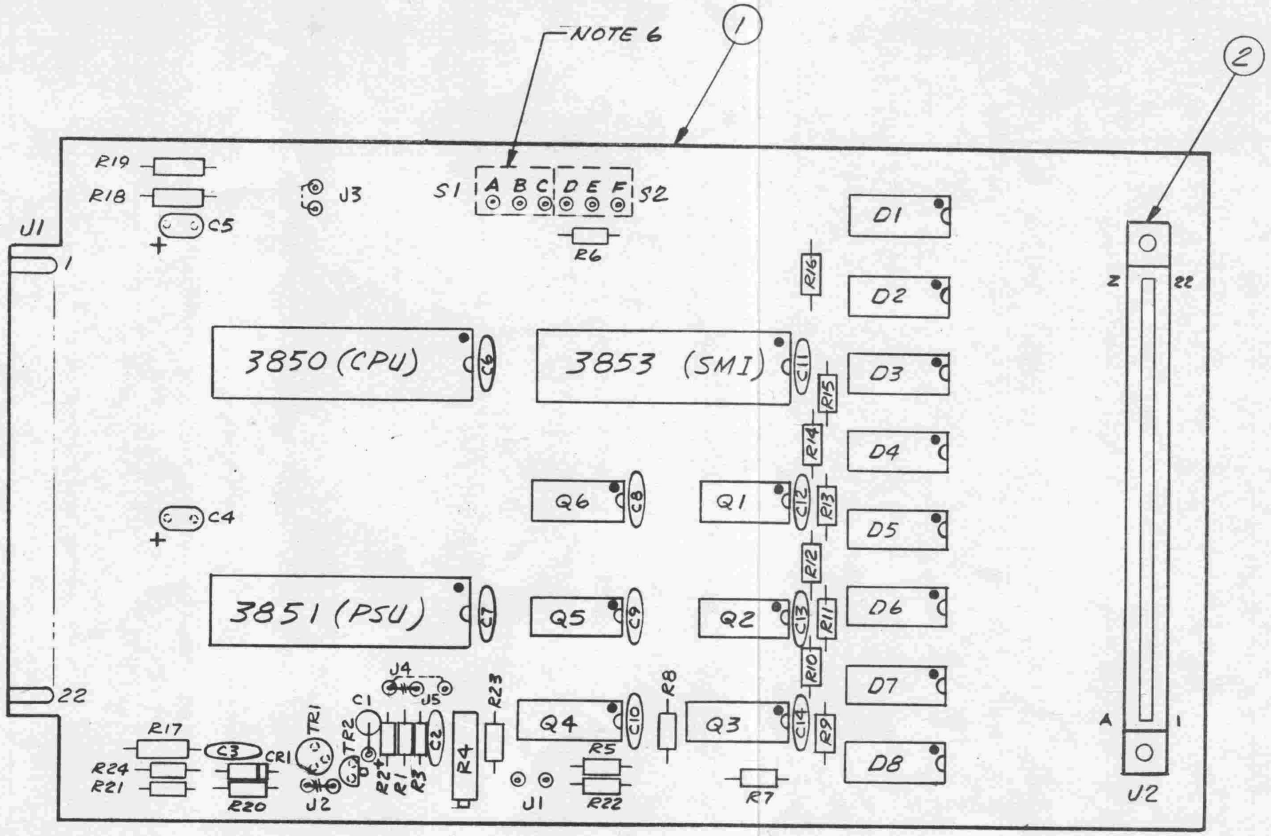
Pin Assignments - Kit Edge Connector

1.	TTY KYBD RTRN	A	+5 volts
2.	TTY PNTR RTRN	B	
3.	I/O 13N	C	I/O o3N
4.	I/O 12 N	D	I/O 02N
5.	I/O 11N	E	I/O 01N
6.	I/O 10N	F	I/O 00N
7.	I/O 17N	H	I/O 07N
8.	I/O 16N	J	I/O 06N
9.	I/O 15N	K	I/O 05N
10.	TTY serial input	L	I/O 14N
11.	I/O o4N	M	TTY PNTR
12.	TTY serial output	N	+12 volts
13.	TTY KYBD	P	I/O 57N
14.	I/O 47N	R	
15.	I/O 40N	S	I/O 50N
16.	I/O 41N	T	I/O 51N
17.	I/O 42N	U	I/O 52N
18.	I/O 43N	V	I/O 53N
19.	I/O 44N	W	I/O 54N
20.	I/O 45N	X	I/O 55N
21.	I/O 46N	Y	I/O 56N
22.		Z	Ground

TABLE 2 (J2)

PIN ASSIGNMENTS- 44 PIN CONNECTOR

1.		A	
2.	D.B.-7	B	D.B.-6
3.	ADD-14	C	ADD -0
4.	P-8	D	ADD-12
5.	P-6	E	D.B.-5
6.	P-7	F	ADD-15
7.	ADD-11	H	DB-7
8.	ADD-5	J	P-5
9.	P-10(READ/WRITE)	K	D.B.-4
10.	ADD-3	L	ADD-2
11.	ADD 10	M	D.B.-3
12.		N	P-4
13.		P	ADD-7
14.		R	ADD-6
15.		S	ADD-8
16.		T	ADD-9
17.		U	P-3
18.		V	D.B.-2
19.		W	
20.	ADD-1	X	P-2
21.	P-1	Y	D.B.-1
22.	D.B.-0	Z	ADD-3



Fairchild / Mostek F8 Evaluation Kit ('F8 KIT 1' Revision C, Sept 25, 1975)

VERAS SYSTEMS CPU BOARD ASSY

PARTS LIST

ITEM NO.	PART IDENT	QTY	ITEM NO.	PART IDENT	QTY	ITEM NO.	PART IDENT	QTY
Q6	4075	1	1	VERAS CPU BD.	1	D1-D8	2102-1<500ns	8
Q5	7406	1	2	CONNECTOR, 22 PIN DUAL	1			
Q3&4	40097	2	C4	47μf/35V TANT	1			
Q1	4001	1	C5	150μf/15V TANT	1			
Q2	4023	1	C6-C14	.05μf/50V DISC	9			
TR1	2N3638	1	R1,3,5,6&8	6.8K, ¼W RES	5			
TR2	2N3904	1	R2,R9-16	22K, ¼W RES	9			
CR1	1N4148	1	R4	35K HELIPOT	1			
C1	4.7μf/35V TANT.	1	R7,21,23&24	3.3K, ¼W RES	4			
C2	10Pf/25V DISC	1	R17-R19	100Ω, ½W RES	3			
C3	.47μf/35V TANT	1	R22	270Ω, ¼W RES	1			

NOTES:

1.) THE CPU BOARD IS SHOWN ASSEMBLED FOR INTERFACING WITH A 20 MA LOOP. IF AN RS-232 INTERFACE IS REQUIRED THEN THE FOLLOWING MODIFICATIONS MUST BE MADE:
(A) CUT JUMPERS J2 & J4 OPEN (B) ADD JUMPER J3 & J5 SHOWN WITH DOTTED LINES ON DWG.
(C) REMOVE R19 (100Ω 1/2W) & REMOVE R20 (1KΩ 1/4W) SUBSTITUTE R20 IN PLACE OF R19.
THE RS-232 SIG RTN IS AT 5 V ABOVE KIT GND, IN SOME CASES IT WILL BE NECESSARY TO "FLOAT" THE KIT PWR SUPPLIES WHEN USING THE RS-232 INTERFACE.

2.) SYSTEM OPERATING SPEED SHOULD BE SET TO 2.0 MHz ±5% (500ns PERIOD) FOR CORRECT TELETYPE OPERATION; ADJUST POT R4 WHILE MONITORING PIN 1 ON THE 3850 CPU.

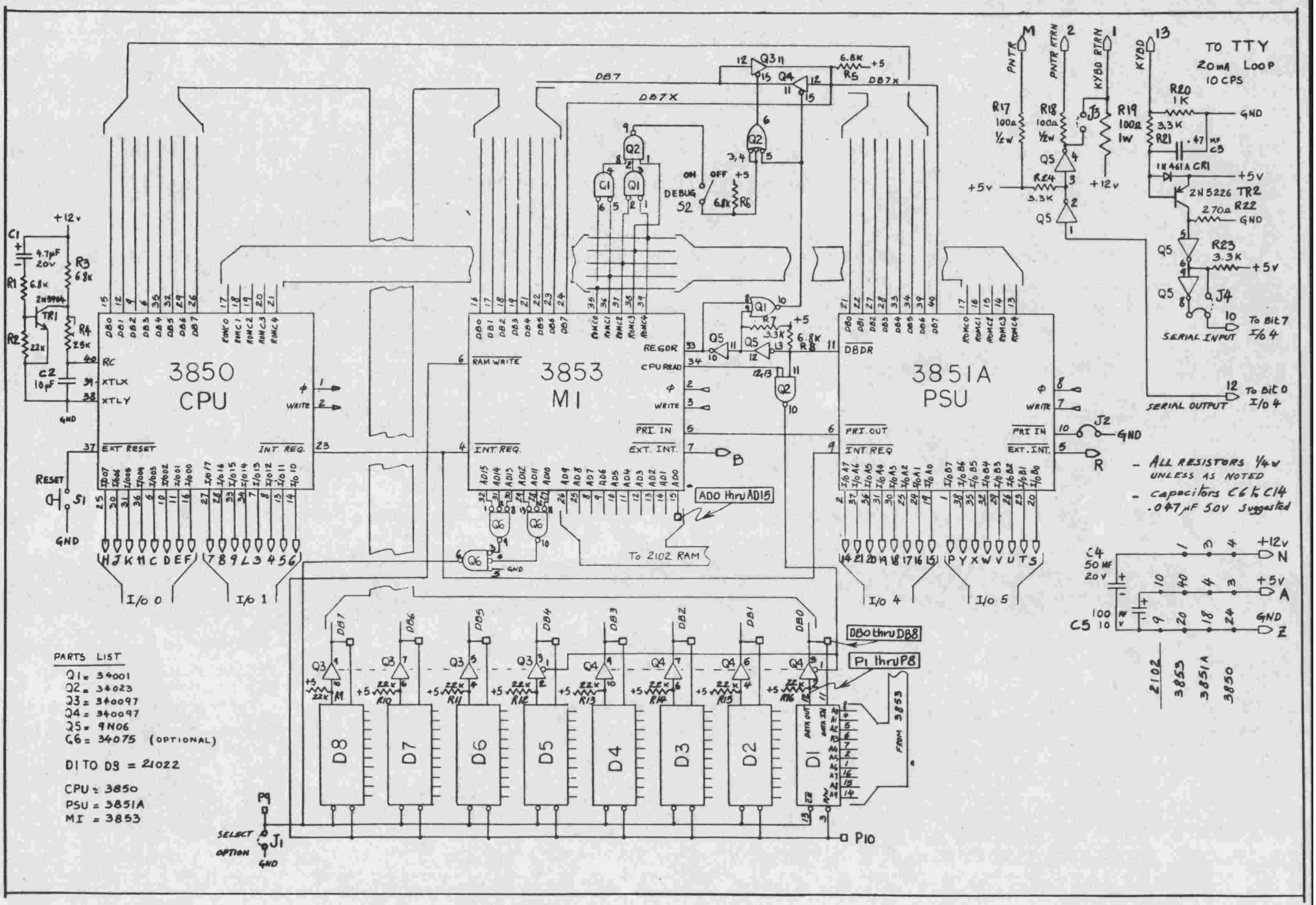
3.) SOME COMPONENTS HAVE BEEN SUBSTITUTED AT VERAS SYSTEMS DISCRETION BUT THIS WILL NOT EFFECT THE PROPER OPERATION OF THE CPU BOARD.

4.) USE OF A LOW POWER SOLDERING IRON & A GOOD GRADE OF 60/40 ELECTRONIC SOLDER IS A MUST.

5.) AFTER ALL COMPONENTS ARE SOLDERED, CHECK FOR SOLDER BRIDGES & COLD SOLDER JOINTS.

6.) IF THE CPU BOARD IS CARD RACK MOUNTED, DO NOT INSTALL S1&S2 (SEE SYSTEMS WIRING DIAG)

7.) ● DENOTES PIN #1 IC ORIENTATION


3850 CPU
3853 MI
3851A PSU
+12v
4.7µF 20v
6.8k
2N3904
22k
25k
GND
RESET
S1
EXT RESET
INT. REQ.
RAM WRITE
REGDR
CPU READ
PRI. IN
EXT. INT.
PRI. OUT
DBDR
WRITE
I/O 0
I/O 1
I/O 4
I/O 5
DB7
DB7X
DEBUG
ON OFF
52
6.8K R6
6.8K R5
DB0 thru DB8
P1 thru P8
ADO thru AD15
To 2102 RAM
SELECT OPTION
J1
P9
P10
PARTS LIST
Q1 = 34001
Q2 = 34023
Q3 = 340097
Q4 = 340097
Q5 = 9N06
C6 = 34075 (OPTIONAL)
D1 TO D8 = 21022
CPU = 3850
PSU = 3851A
MI = 3853
TO TTY
20mA Loop
10 CPS
PNTR
PNTR RTRN
KYBD RTRN
KYBD
R17 100Ω ½W
R18 100Ω ½W
R19 100Ω 1W
R20 1K
3.3K
R21 .47 MF C3
1N461A CR1
2N5226 TR2
270Ω R22
R23 3.3K
R24 3.3K
J3
J4
J2
To Bit 7 I/O 4
SERIAL INPUT
To Bit 0 I/O 4
SERIAL OUTPUT
- ALL RESISTORS ¼W UNLESS AS NOTED
- Capacitors C6 & C14 .047µF 50V Suggested
C4 50 MF 20V
C5 100 MF 10V
+12v N
+5v A
GND Z
2102
3853
3851A
3850